

# Thermal Test Chip for Thermal Characterization and Qualification of Materials and Semiconductor Packages

44<sup>th</sup> Symposium & Exposition

Boxboro Regency Hotel & Conference Center, Boxborough MA USA

Mohamad Abo Ras and Dave Saums

02 May 2017



# NANOTEST

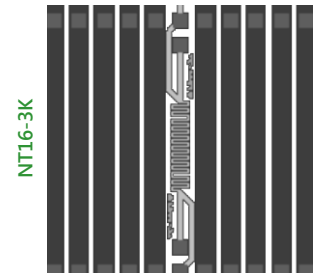
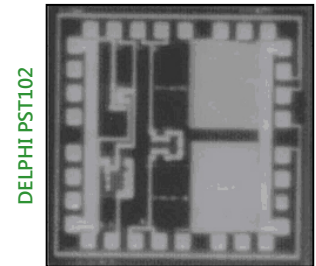
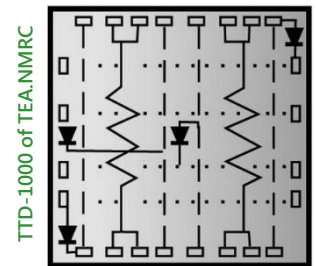
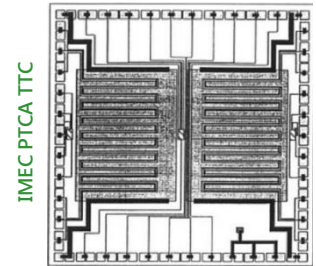
Berliner Nanotest und Design GmbH

In cooperation with



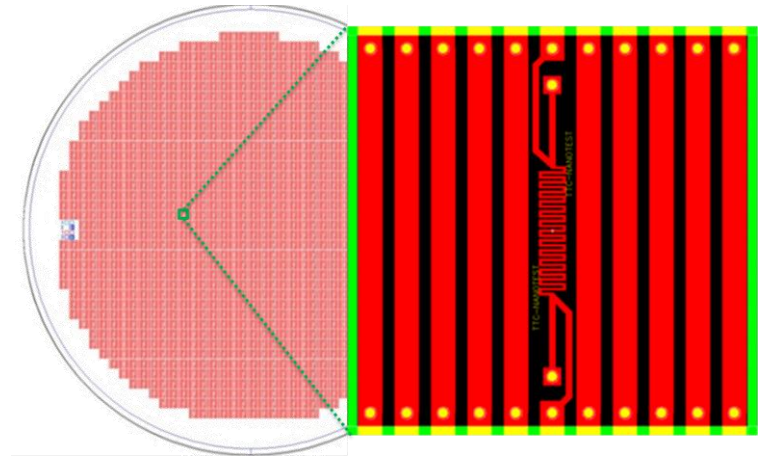
- Motivation
- Design of the Thermal Test Chip
- Qualification and Calibration
- Application examples
  - » Material characterization at TIMA™
  - » Material characterization at TransTIMA™
  - » Highly conductive die attach characterization
  - » Load profile generation
  - » Optical reference heat source
  - » Fluidic analysis
- Conclusion & Outlook

- What is a Thermal Test Chip (TTC)?
  - » Basic chip for testing and characterization
  - » Each consists of:
    - a heat source
    - a temperature sensor
    - contacting pads
- Why did we create an own Thermal Test Chip?
  - » Limited availability and selection of TTCs on the market
  - » Available chips do not fulfill requirements:
    - Low power density
    - Inhomogeneous heat dissipation
    - Low temperature accuracy
  - » TTCs are the mainly used tool for thermal characterization and qualification of materials and packages in electronics
  - » A gap in the market



- Modularity
  - » Different chip sizes available to meet most requirements
- Homogeneity
  - » Uniform heater structures for homogeneous heat dissipation up to  $1 \text{ W/mm}^2$
- Resolution
  - » Thermal resolution of temperature sensing up to  $\pm 0.2 \text{ K}$
  - » Spatial resolution of temperature sensing up to  $\pm 500 \mu\text{m}$
- Reliability
  - » Suitable for long-term load cycle testing to  $> 100,000$  cycles
- Cost-Effectiveness
  - » Suitable as consumable rather than as invest
- Assembly
  - » Available for different assembling technologies
- Metallization
  - » Available with different backside metallization

- Wafer
  - » Standard 150 mm Si wafer
  - » Thickness
    - Bulk silicon: 675  $\mu\text{m}$
    - Oxide coating: 1  $\mu\text{m}$
  - » 1200 chips per wafer



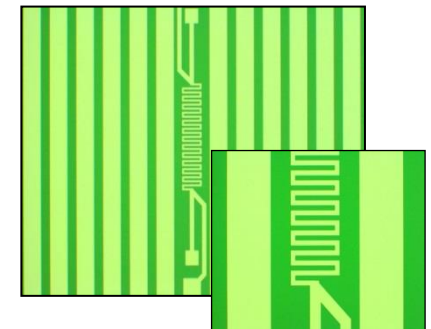
- Masks

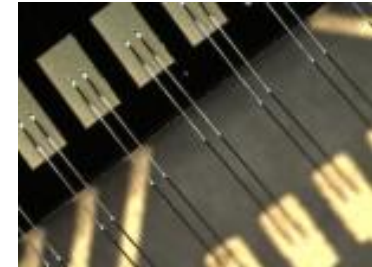
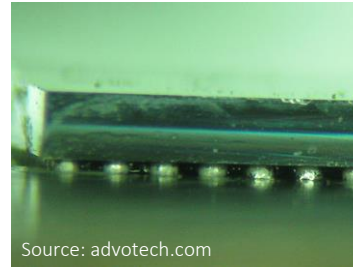
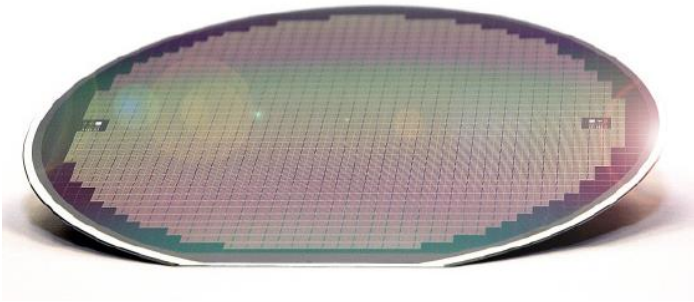
- » **Use of only 3 masks for the full process:**

1. Mask for lithography of the temperature sensor and heater structures
2. Mask to open the vias for contacting the structures
3. Mask for the deposition of the contact layer metallization

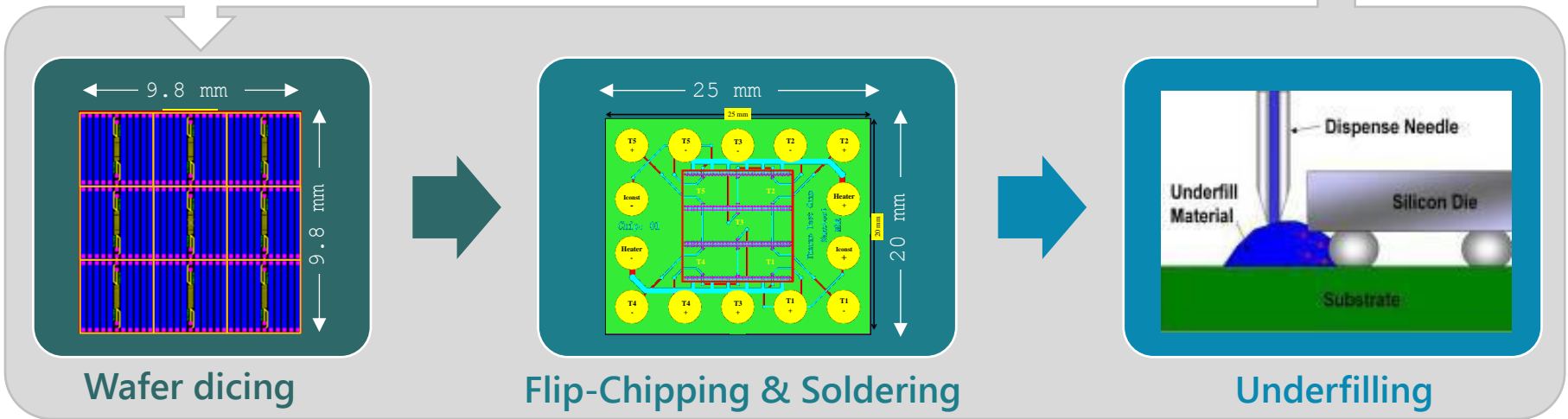
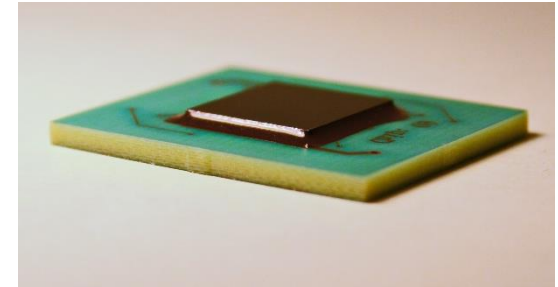
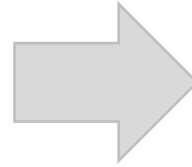
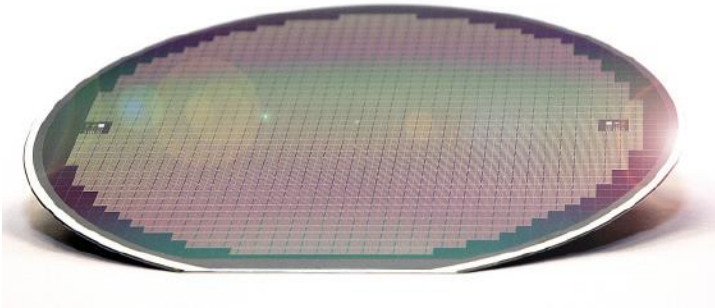
- The Edge

- » Few masks for the whole process
  - » Si wafers in standard size
  - » Processing steps with small tolerances
  - » Fully modular wafer layout for custom chip sizes





Assembling technology	Flip Chip Assembly	Wirebond Assembly
Fabrication technology	Thin film	Thin film
Wafer diameter	150 mm	150 mm
Wafer thickness	<b>675 μm</b>	<b>400 μm</b>
Cell size	3.2 x 3.2 mm <sup>2</sup>	3.2 x 3.2 mm <sup>2</sup>
Cell count	1200	1200
Heaters per cell	10 resistors (160 Ω each)	10 resistors (160 Ω each)
Sensors per cell	1 resistor (3 kΩ each @ RT)	1 resistor (3 kΩ each @ RT)
Backside metallization	<b>None</b>	<b>Ti/Pt/Au (100 nm each)</b>
Contact pad	<b>Cu pillar (40 μm) &amp; AgSn (30 μm)</b>	<b>Al metallization</b>
Pad size	<b>80 μm</b>	<b>150 μm</b>
Pad raster	300 μm	300 μm

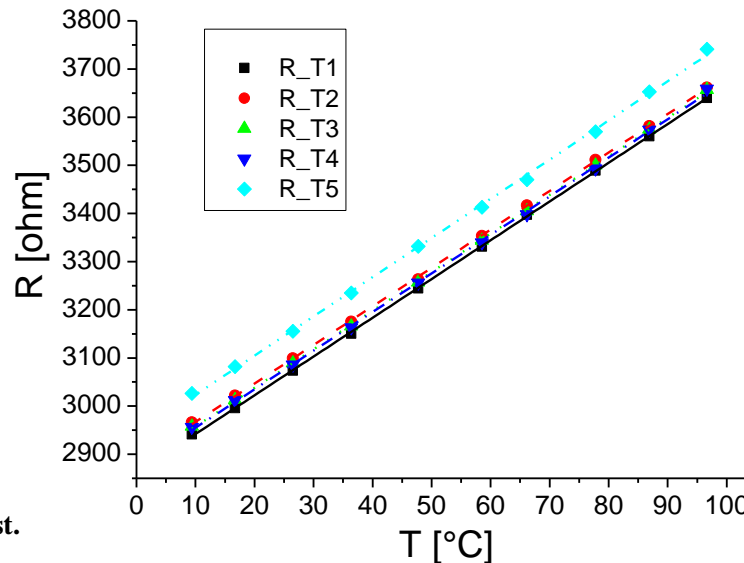
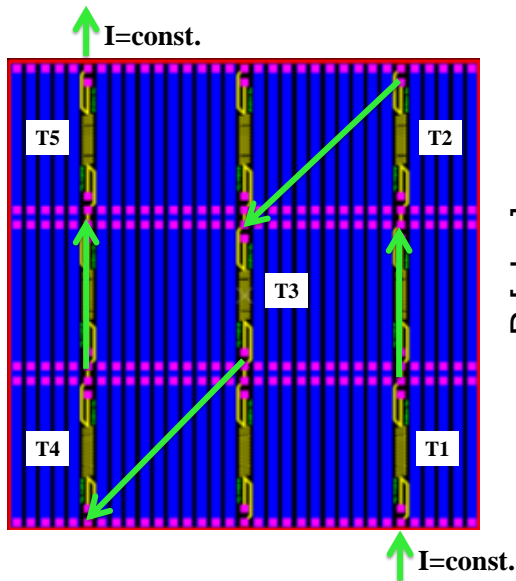


- Standard semiconductor process with low defect rate
- Default package for Nanotest applications:
  - » Full-area heater and five temperature sensors
- Highly reliable package that is suited for cycle testing

- Calibration with Nanotest HK200™
- Calibration of 5 sensors simultaneously
- Four-wire termination
  - » 1 mA sensing current
- Resistance perfectly proportional to the temperature
  - »  $R^2 > 0.9998$



Nanotest HK200™



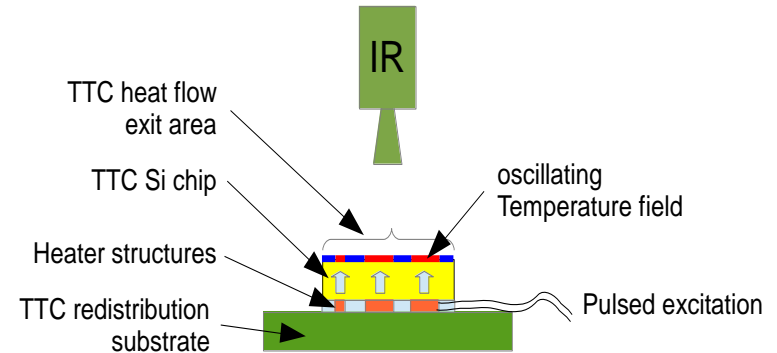
#	Slope [Ω/K]	axis intercept [Ω]
T1	8,049	2861
T2	7,994	2887
T3	8,013	2878
T4	8,009	2875
T5	8,140	2942
mean	8,041	2889

**sensitivity: 8 Ω/K**

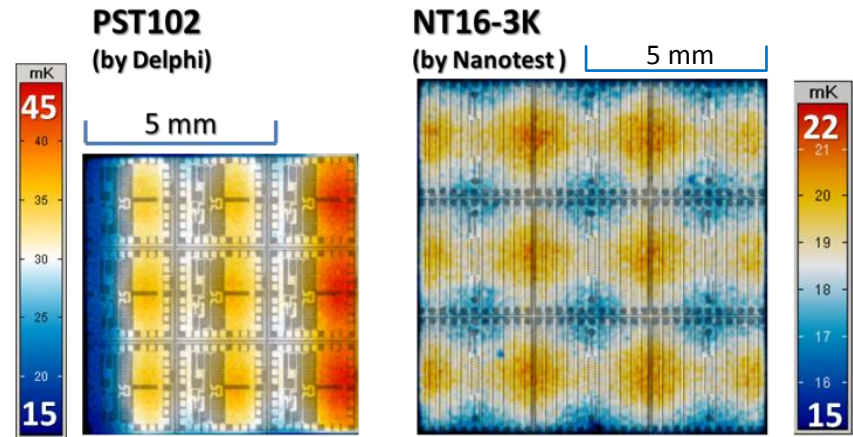
→ **4X higher sensitivity** compared to Si diodes (@ 1 mA)



- Homogeneity is of very high importance for TIM characterization:
  - » Inhomogeneous heat flow leads to faulty thermal analysis results
- Use of thermal imaging for transient modulated technique
  - » At steady-state ( $Q = 0$ ), non-homogeneities are not detectable
- Lock-in thermography amplitude image for quantification of the heat flow distribution



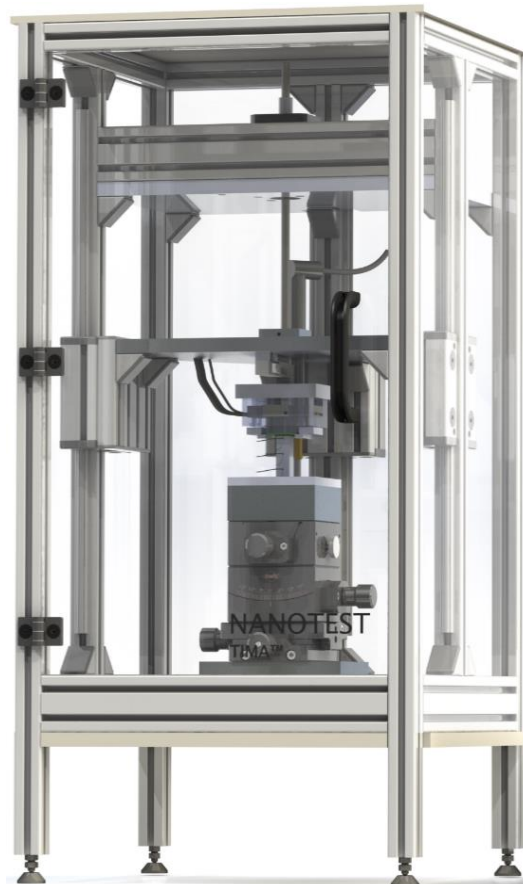
**NT16-3K is a 4X improvement over earlier test die previously used in thermal characterization.**



## TIMA™

### Steady state measurement technique

- Measurement of bulk thermal **conductivity** of low to medium thermally conductive material
- Measurement of thermal **interface** resistances
- For solid and viscous materials
  - » Substrates (FR4, IMS, LTCC, HTCC etc.)
  - » TIMs (greases, adhesives, gap fillers, films etc.)
  - » Isolation layers (foils, foams etc.)
- Cyclic testing for **ageing** investigations
  - » Thermal and/or mechanical cycling
- Advanced **customized** thermal investigations



Selection of feasible samples

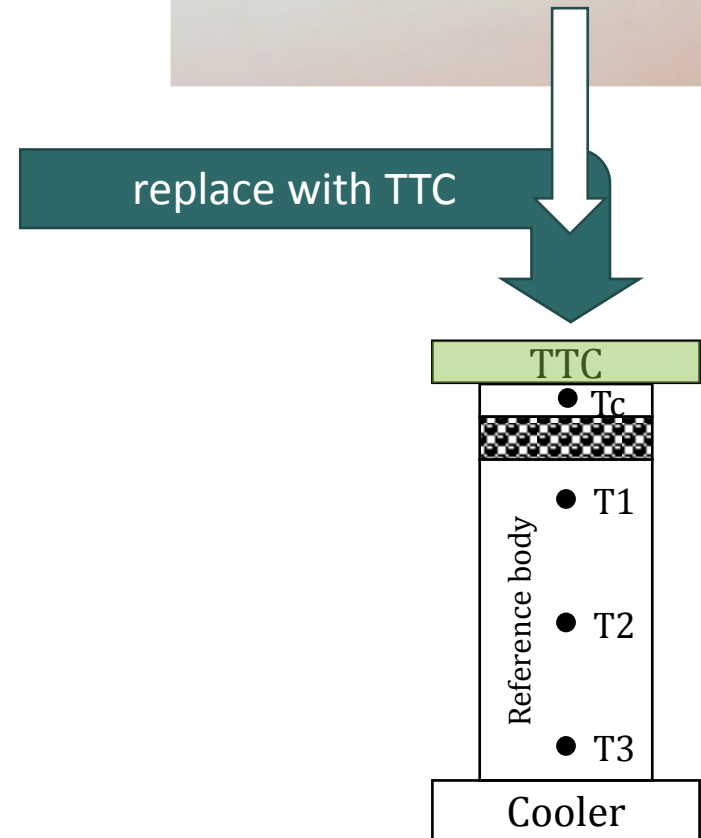
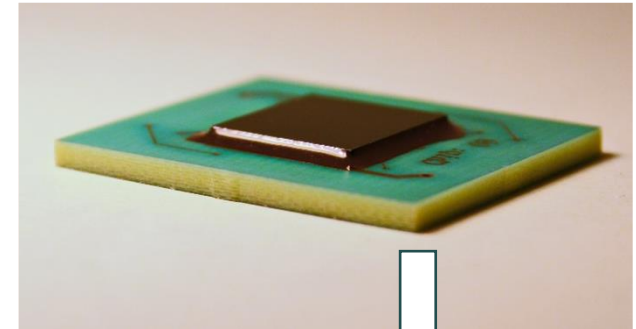
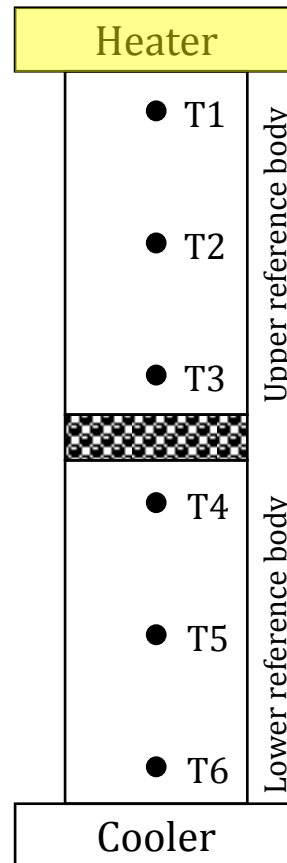
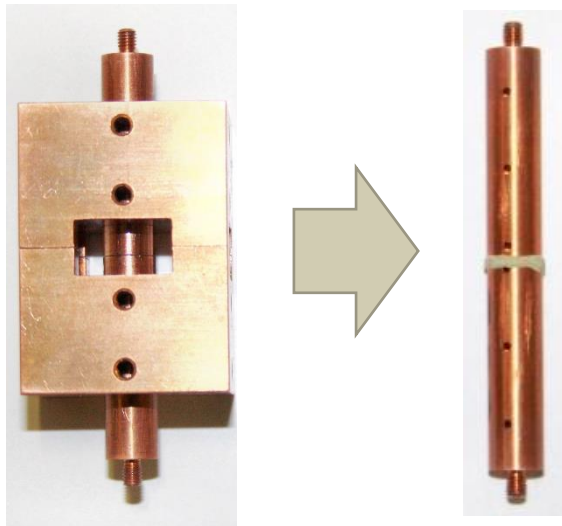
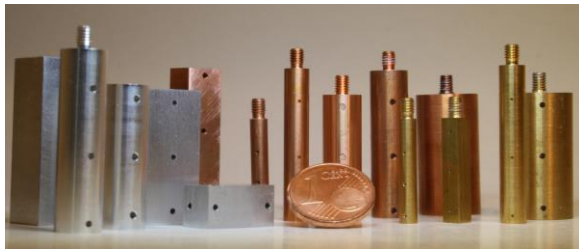


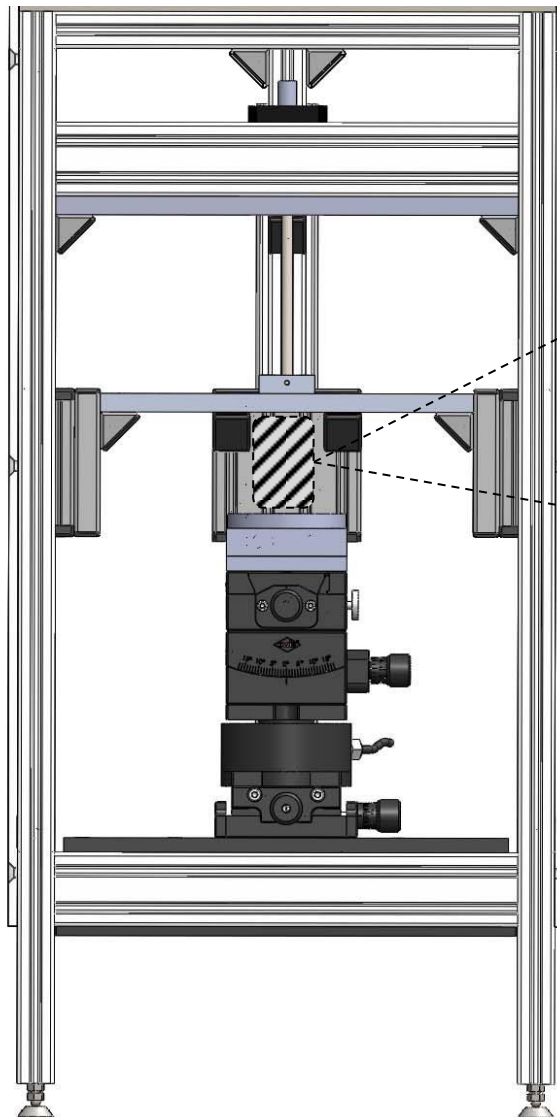
Selection of metal test heads for characterization



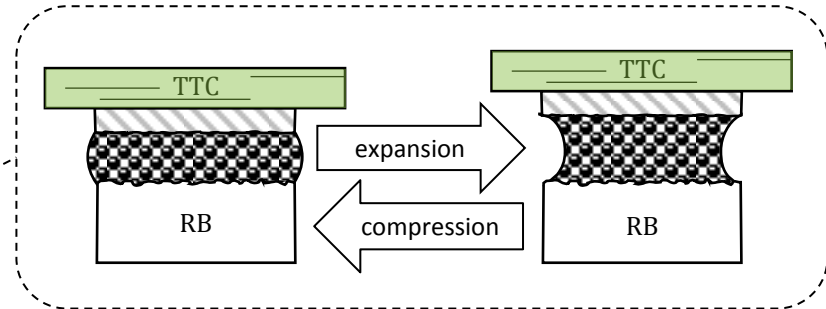
All-round steady-state characterization platform

- Method based on ASTM D-5470
  - » Advanced studies with die surface

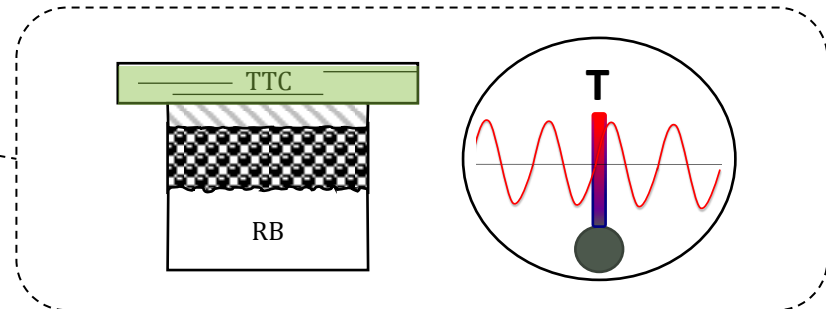




## Mechanical loading



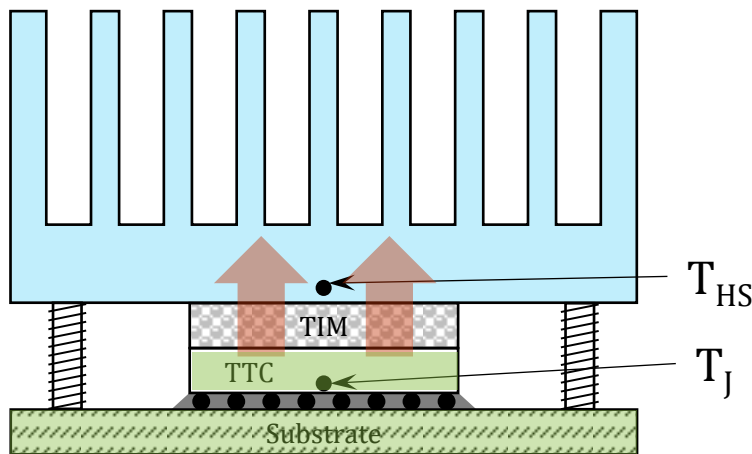
Combined loading



## Thermal loading

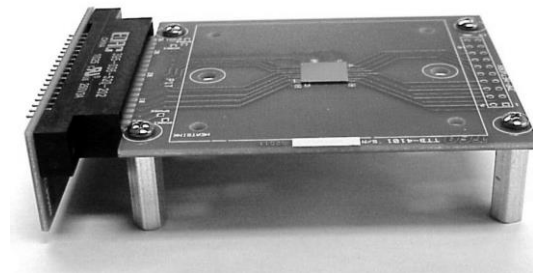
- » Mechanical or thermal cycling
- » Combined loading
- » In-situ measurement of BLT and pressure
- » In-situ measurement of thermal resistance
- » Computer-controlled long term testing
- » **Sophisticated ageing studies**

- Implementation of the JEDEC standard JESD51-3
  - » Determination of the effective thermal resistance of TIMs
  - » In-situ and ex-situ investigation of ageing behavior
- Highly compact, affordable and easy to build

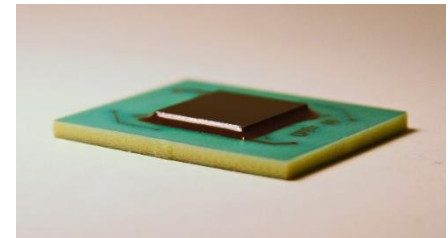


schematic of method

$$R_{th} = \frac{T_J - T_{HS}}{\dot{Q}}$$

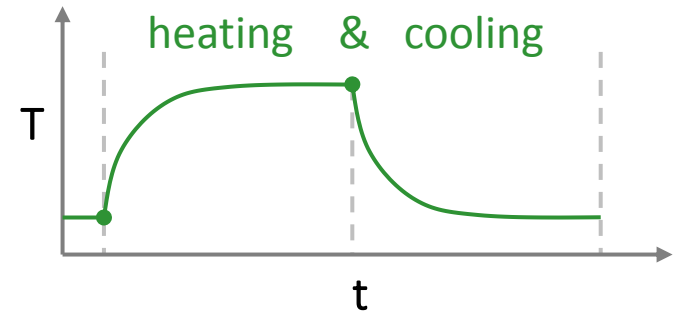
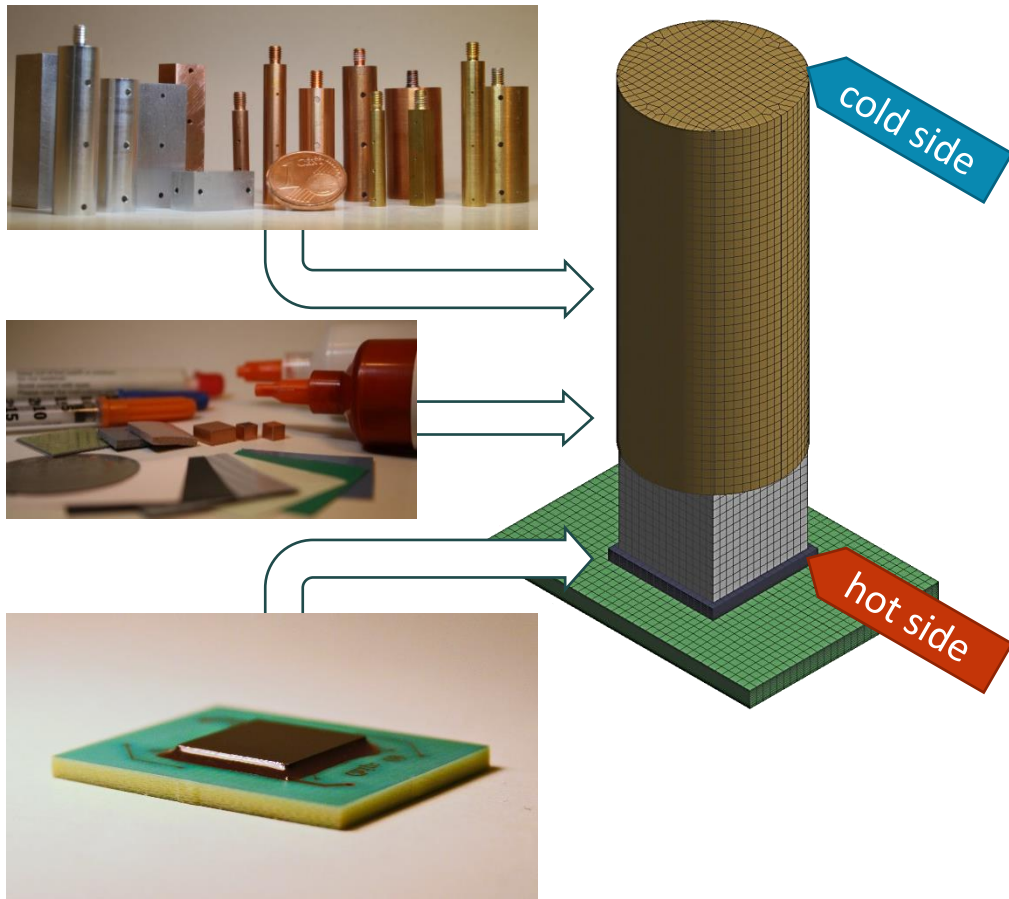


TTV-410X by TEA

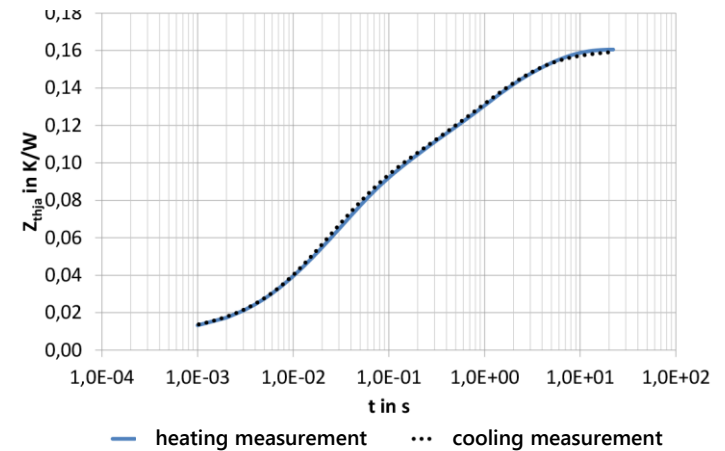


TTV by NANOTEST

- Combination of TIMA™ and thermal transient methods
  - » **The edge of the TTC:** separation of heating and sensing allows for temperature measurement regardless of the power state



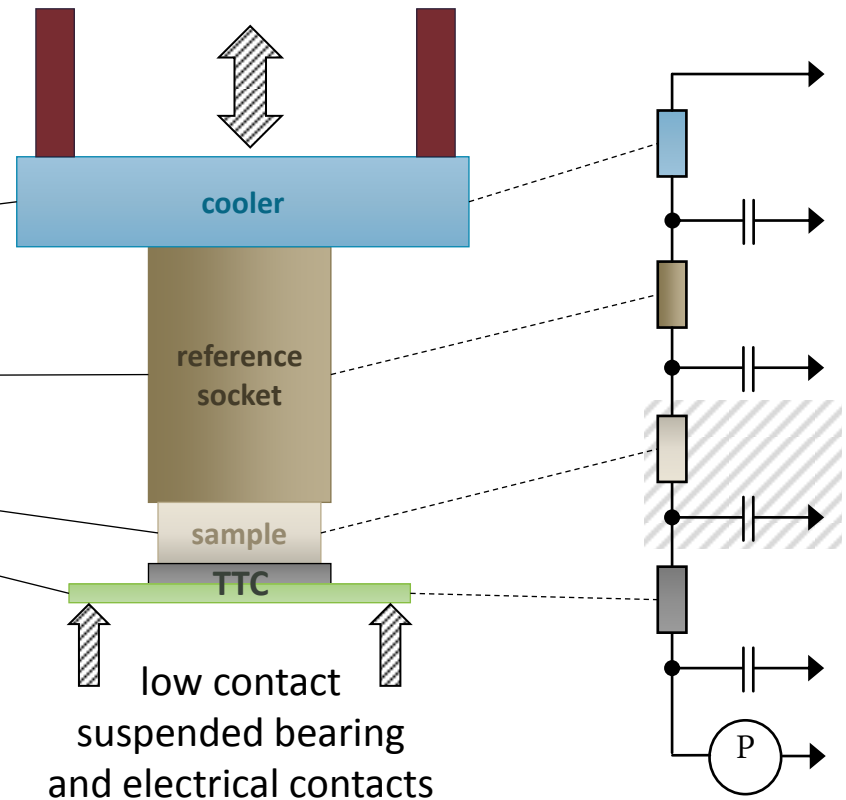
Zth(t) curves from heating and cooling in comparison

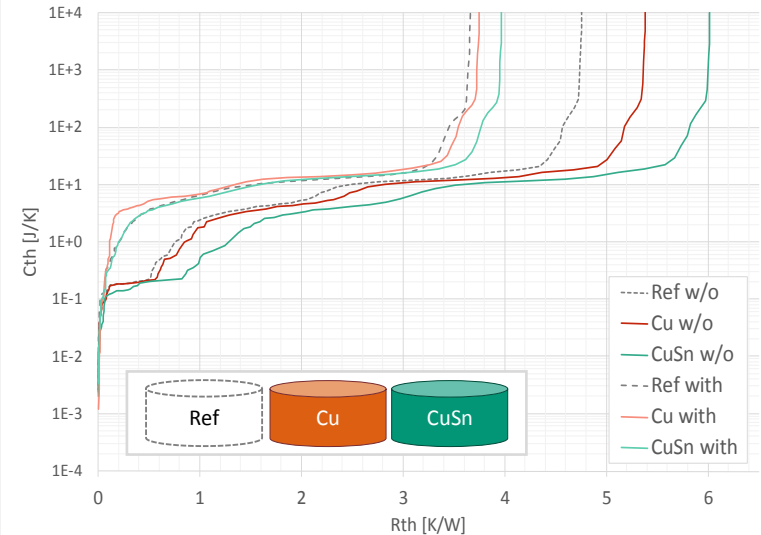
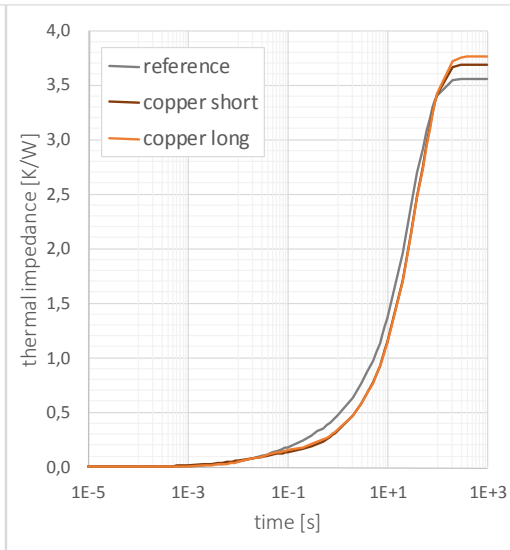
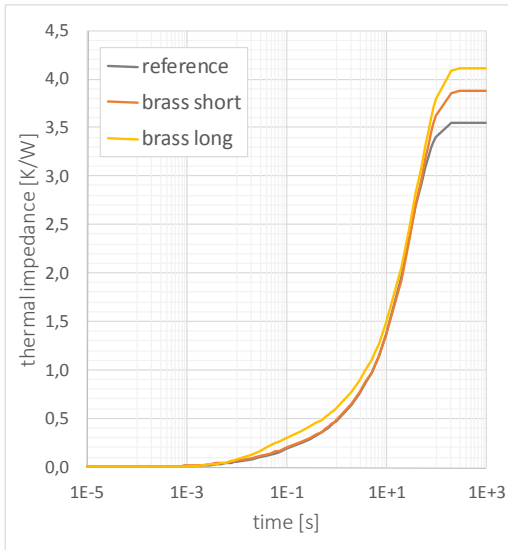




(Source: PhD. Alexander Hensler)





- Determination of a thermal equivalent network model
- Numerical analysis for determination of thermal properties of sample layer
- Derived from JEDEC JESD51-14





#	$R_{th,J-A}$ [K/W]
	3,58
	3,88
	4,12

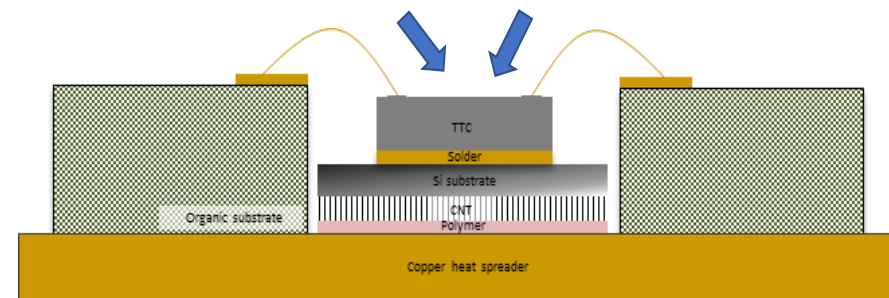
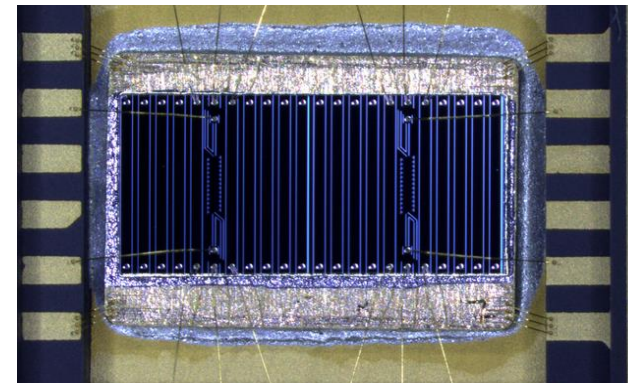
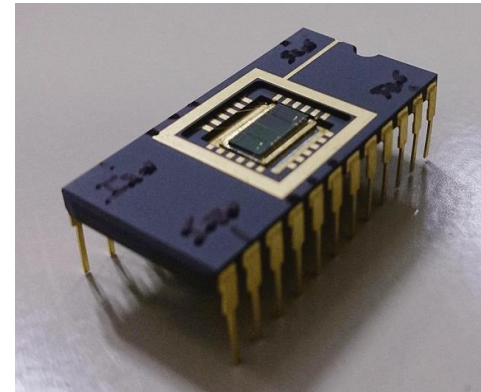
#	$R_{th,J-A}$ [K/W]
	3,58
	3,68
	3,76

- Metal samples -- evaluation study (published at IMAPS France ATW Thermal, La Rochelle FR 2016)
- Structure function for detailed analysis on multilayer-samples

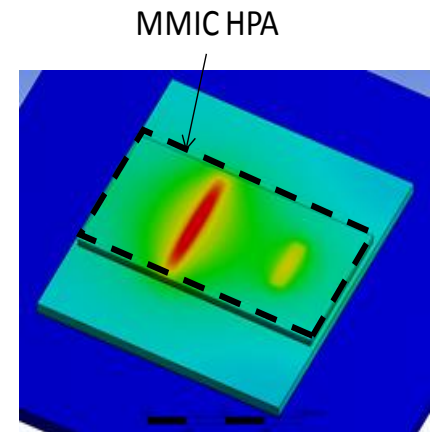
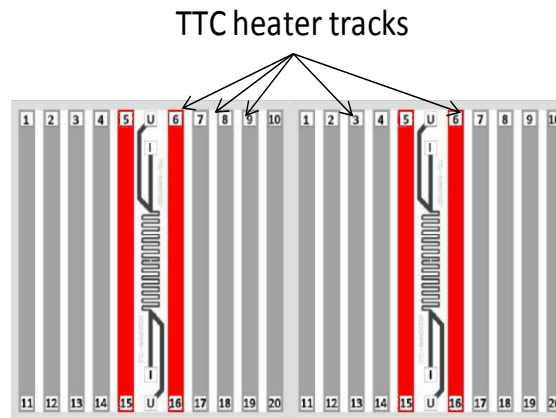
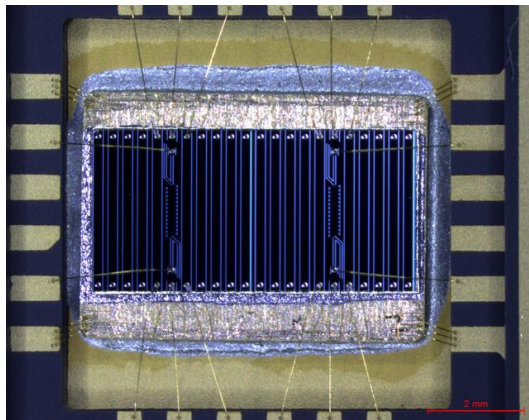
- » Highly compact and efficient tool for transient thermal characterization of thermal interface materials
- » Directly application related results, determined with direct contact to die surface.



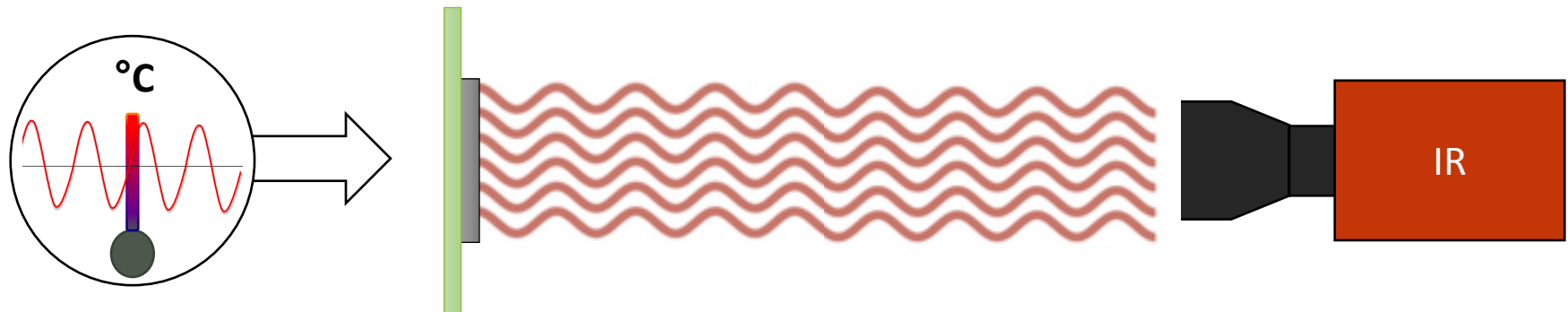
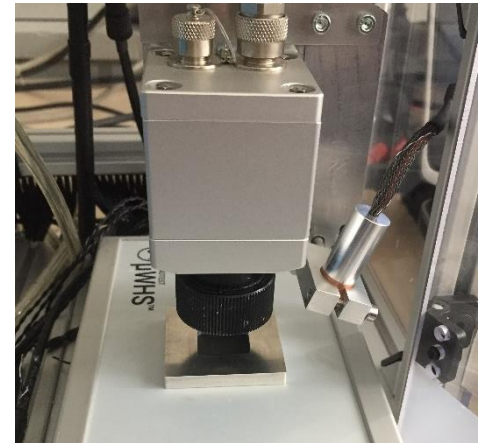
- Characterization of vertically aligned carbon nanotubes (VACNTs)
- TTC as replacement for the real application target chip
- Used for excitation (heating) and temperature sensing
- Measurement of the transient step response
- Comparison to reference measurement with standard adhesive



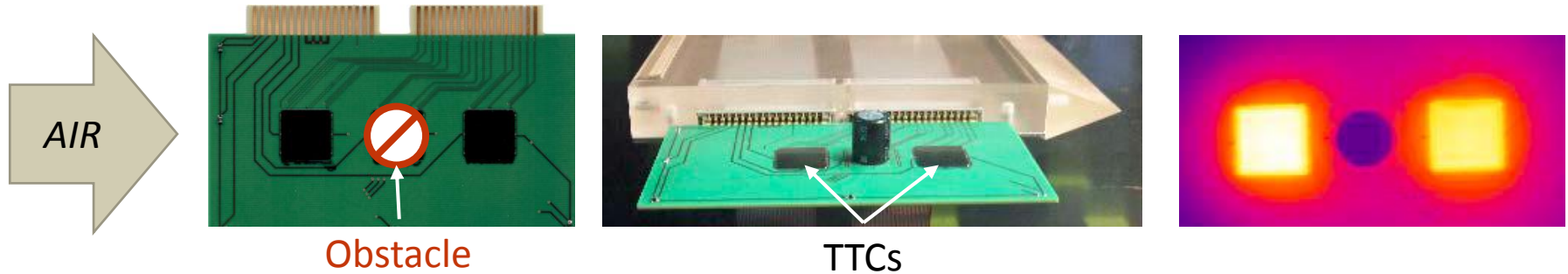
- Separate contacting of heater lanes allows recreation of various custom load profiles
- Heater lanes can be individually contacted and controlled to generate
  - » Custom hot spots
  - » Defined temperature gradients / fields
  - » Application case-specific heat density distributions can be incorporated in testing



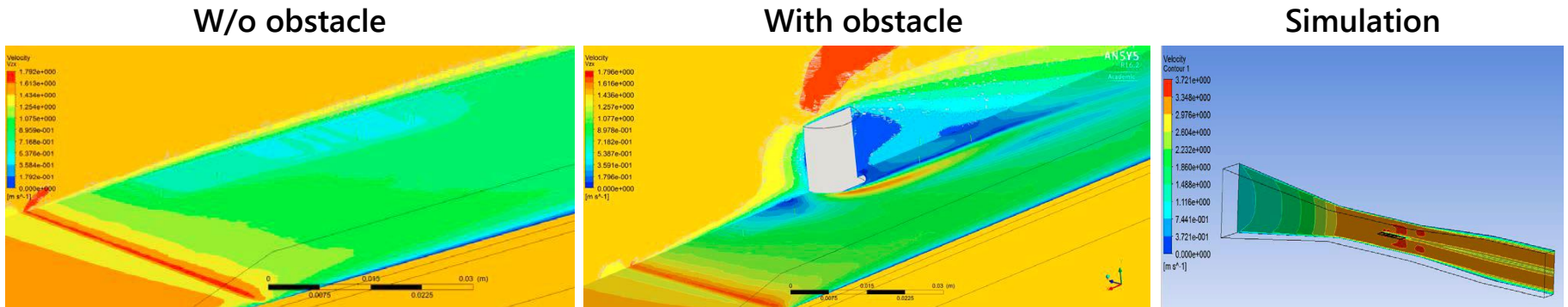
- Chip-surface ideal for reference measurements close to application
  - » Coatable with any metal / material of choice
  - » Reflecting (native) or matte (camera paint)
- Multiple purposes
  - » Infrared & thermoreflectance thermography
  - » Controlled and precise temperature reference
    - Homogeneous or temperature gradients
  - » Time-domain for lock-in analysis



- Influence of obstacles in air flow on active air cooling
- Two TTCs in air flow direction with obstacle in between



- TTC as both heat source and temperature sensor



- Good correlation between simulation and experiment

- Available TTCs did not fully meet our requirements
  - » *Very* limited availability and/or quality.
- We created a TTC that meets our requirements:
  - » High precision, suited for accurate thermal characterization
  - » Available for different assembly and packaging technologies
  - » Highly configurable and flexible
- Numerous different application examples prove the diverse feasibility and flexibility of these TTCs:
  - » In-situ material and system characterization
  - » May be used for both transient and steady-state analyses
  - » Optical calibration or referencing is practicable
  - » Capable for use in sophisticated analyses and complex studies

## **Berliner Nanotest und Design GmbH**

Volmerstrasse 9B  
12489 Berlin Germany



Mohamad Abo Ras, CEO, Co-founder

Email: [aboras@nanotest.eu](mailto:aboras@nanotest.eu)

Tobias von Essen, R&D

Email: [vonessen@nanotest.eu](mailto:vonessen@nanotest.eu)

Web: [www.nanotest.eu](http://www.nanotest.eu)

Tel: +49 30 6392 3614

## **DS&A LLC**

Collaborative Innovation Works  
11 Chestnut Street  
Amesbury MA 01913 USA



Dave Saums, Principal

Email: [dsaums@dsa-thermal.com](mailto:dsaums@dsa-thermal.com)

Web: [www.dsa-thermal.com](http://www.dsa-thermal.com)

Tel: 1 978 499 4990

